ABSTRACT OF THE DISCLOSURE

A method and apparatus for converting a full-rate digital clock circuit to a fractional-rate clock circuit. The combinatorial and sequential functions of the full rate design are duplicated, with a first combinatorial function responsive to even input logic vectors and a second combinatorial function responsive to odd input logic vectors. Output vectors from the first and the second combinatorial function are provided as input vectors to the respective first and second sequential function, which operate at a fractional clock rate and provide the output block vectors.